

## FDC5612

# 60V N-Channel PowerTrench® MOSFET

### **General Description**

This N-Channel MOSFET has been designed specifically to improve the overall efficiency of DC/DC converters using either synchronous or conventional switching PWM controllers.

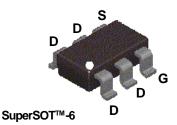
These MOSFETs feature faster switching and lower gate charge than other MOSFETs with comparable  $R_{\rm DS(ON)}$  specifications.

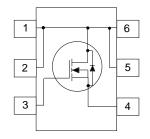
The result is a MOSFET that is easy and safer to drive (even at very high frequencies), and DC/DC power supply designs with higher overall efficiency.

### **Features**

• 4.3 A, 60 V. 
$$R_{DS(ON)} = 0.055~\Omega~$$
 @  $V_{GS} = 10~V$   $R_{DS(ON)} = 0.064~\Omega~$  @  $V_{GS} = 6~V$ 

- Low gate charge (12.5nC typical).
- Fast switching speed.
- $\bullet \;\;$  High performance trench technology for extremely low  $R_{\mbox{\tiny DS(ON)}}.$
- SuperSOT™-6 package: small footprint (72% smaller than standard SO-8); low profile (1mm thick).





Absolute Maximum Ratings T<sub>A</sub> = 25°C unless otherwise noted

Symbol	Parameter		Ratings	Units
V <sub>DSS</sub>	Drain-Source Voltage		60	V
$V_{GSS}$	Gate-Source Voltage		<u>+</u> 20	V
I <sub>D</sub>	Drain Current - Continuous	(Note 1a)	4.3	Α
	Drain Current - Pulsed		20	
P <sub>D</sub>	Power Dissipation for Single Operation	(Note 1a)	1.6	W
		(Note 1b)	0.8	
$T_J,T_stg$	Operating and Storage Junction Temperature Range		-55 to +150	°C

**Thermal Characteristics** 

$R_{\theta^{JA}}$	Thermal Resistance, Junction-to-Ambient	(Note 1a)	78	∘C/W
R <sub>OJC</sub>	Thermal Resistance, Junction-to-Case	(Note 1)	30	°C/W

**Package Outlines and Ordering Information** 

Device Marking	Device	Reel Size	Tape Width	Quantity
.562	FDC5612	7"	8mm	3000 units

Symbol	Parameter	Test Conditions	Min	Typ	Max	Units
Off Char	racteristics					
BV <sub>DSS</sub>	Drain-Source Breakdown Voltage	$V_{GS} = 0 \text{ V}, I_{D} = 250 \mu\text{A}$	60			V
ΔBVDSS ΔTJ	Breakdown Voltage Temperature Coefficient	$I_D = 250 \mu A$ , Referenced to 25°C		58		mV/∘C
I <sub>DSS</sub>	Zero Gate Voltage Drain Current	$V_{DS} = 48 \text{ V}, V_{GS} = 0 \text{ V}$			1	μA
I <sub>GSSF</sub>	Gate-Body Leakage Current, Forward	V <sub>GS</sub> = 20 V, V <sub>DS</sub> = 0 V			100	nA
I <sub>GSSR</sub>	Gate-Body Leakage Current, Reverse	V <sub>GS</sub> = -20 V, V <sub>DS</sub> = 0 V			-100	nA
On Char	racteristics (Note 2)					
$V_{GS(th)}$	Gate Threshold Voltage	$V_{DS} = V_{GS}, I_{D} = 250  \mu A$	2	2.2	4	V
$\frac{\Delta VGS(th)}{\Delta T_J}$	Gate Threshold Voltage Temperature Coefficient	$I_D$ = 250 $\mu$ A, Referenced to 25°C		-5.5		mV/°C
R <sub>DS(on)</sub>	Static Drain-Source On-Resistance	$V_{GS} = 10 \text{ V}, I_D = 4.3 \text{ A}$ $V_{GS} = 10 \text{ V}, I_D = 4.3 \text{ A}, T_J = 125 ^{\circ}\text{C}$ $V_{GS} = 6 \text{ V}, I_D = 4 \text{ A}$		0.042 0.072 0.048	0.055 0.094 0.064	Ω
I <sub>D(on)</sub>	On-State Drain Current	V <sub>GS</sub> = 10 V, V <sub>DS</sub> = 5 V	10			Α
<b>g</b> <sub>FS</sub>	Forward Transconductance	$V_{DS} = 10 \text{ V}, I_{D} = 4.3 \text{ A}$		14		S
Dvnamio	Characteristics					
C <sub>iss</sub>	Input Capacitance	V <sub>DS</sub> = 25 V, V <sub>GS</sub> = 0 V,		650		pF
Coss	Output Capacitance	f = 1.0 MHz 80 35			pF	
C <sub>rss</sub>	Reverse Transfer Capacitance			35		pF
Switchin	ng Characteristics (Note 2)					
t <sub>d(on)</sub>	Turn-On Delay Time	$V_{DD} = 30 \text{ V}, I_D = 1 \text{ A},$		11	20	ns
t <sub>r</sub>	Turn-On Rise Time	$V_{GS} = 10 \text{ V}, R_{GEN} = 6 \Omega$		8	18	ns
t <sub>d(off)</sub>	Turn-Off Delay Time			19	35	ns
t <sub>f</sub>	Turn-Off Fall Time			6	15	ns
Q <sub>g</sub>	Total Gate Charge	$V_{DS} = 30 \text{ V}, I_{D} = 4.3 \text{ A},$		12.5	18	nC
Q <sub>gs</sub>	Gate-Source Charge	V <sub>GS</sub> = 10 V		2.4		nC
$Q_{gd}$	Gate-Drain Charge			2.6		nC
Drain-Sc	ource Diode Characteristics and	d Maximum Ratings				
l <sub>s</sub>	Maximum Continuous Drain-Source Did				1.3	Α
V <sub>SD</sub>	<del>†</del>	I		l —		V

R<sub>QJA</sub> is the sum of the junction-to-case and case-to-ambient resistance where the case thermal reference is defined as the solder mounting surface of the drain pins. R<sub>QJC</sub> is guaranteed by design while R<sub>QCA</sub> is determined by the user's board design.

 a) 78 °C/W when mounted on a 1.0 in² pad of 2 oz. copper.

b) 156 °C/W when mounted on a minimum pad.

<sup>2.</sup> Pulse Test: Pulse Width £ 300 ms, Duty Cycle £ 2.0%

### **Typical Characteristics**

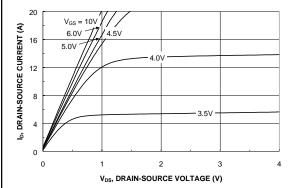


Figure 1. On-Region Characteristics.

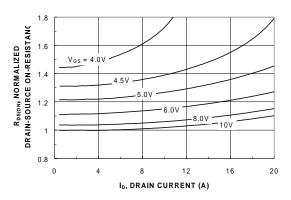


Figure 2. On-Resistance Variation with Drain Current and Gate Voltage.

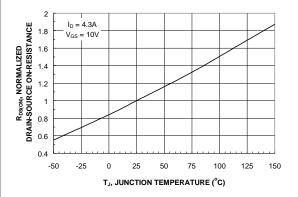


Figure 3. On-Resistance Variation with Temperature.

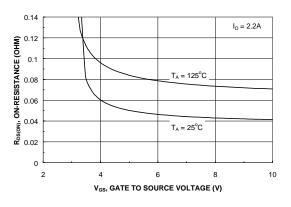


Figure 4. On-Resistance Variation with Gate-to-Source Voltage.

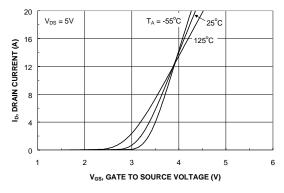


Figure 5. Transfer Characteristics.

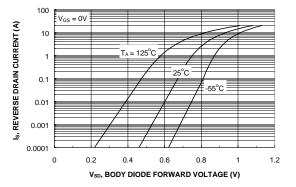
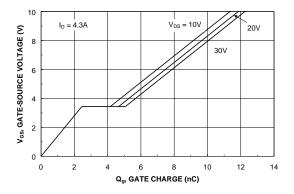


Figure 6. Body Diode Forward Voltage Variation with Source Current and Temperature.

### **Typical Characteristics**



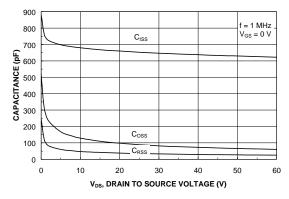


Figure 7. Gate Charge Characteristics.

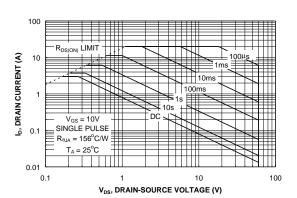


Figure 8. Capacitance Characteristics.

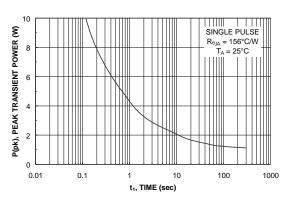


Figure 9. Maximum Safe Operating Area.



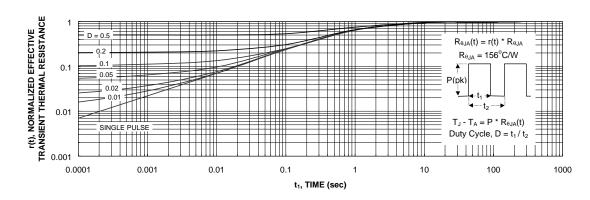


Figure 11. Transient Thermal Response Curve.

Thermal characterization performed using the conditions described in Note 1b. Transient thermal response will change depending on the circuit board design.

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